# AT91RM9200 Microcontroller Schematic Check List

## 1. Introduction

This application note is a schematic review check list for systems embedding the Atmel® ARM® Thumb®-based AT91RM9200 microcontroller.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91RM9200. This document does not consider PCB layout constraints.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb Microcontrollers

Application Note

6323A–ATARM–03-Jul-07

## 2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91RM9200 Microcontroller on Atmel's Web site.

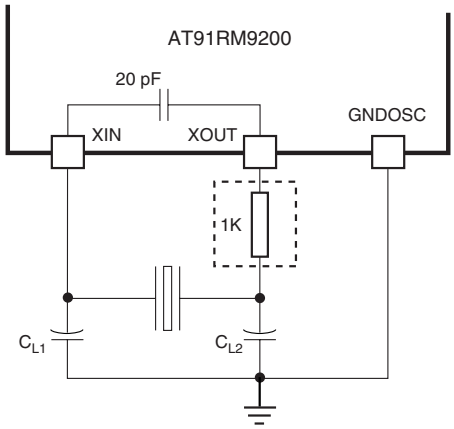
Table 2-1 gives the associated documentation needed to support full understanding of this application note.

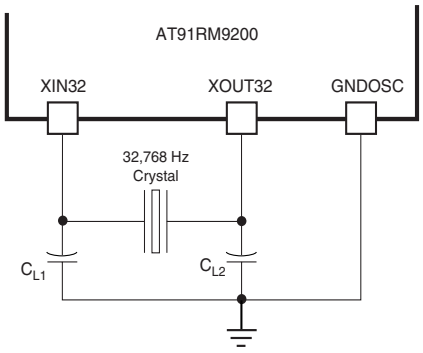
**Table 2-1.** Associated Documentation

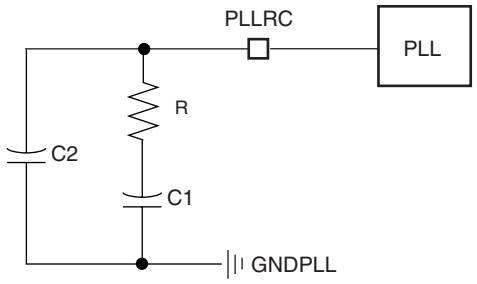
| Information | Document Title |
|---|---|
| User Manual<br>Electrical/Mechanical Characteristics<br>Ordering Information<br>Errata | AT91RM9200 Product Datasheet |
| Internal architecture of processor<br>ARM/Thumb instruction sets<br>Embedded in-circuit-emulator | ARM9TDMI® Technical Reference Manual<br>ARM920T™ Technical Reference Manual |
| Evaluation Kit User Guide | AT91RM9200-EK Evaluation Board User Guide |

## 3. Schematic Check List

| ☑ | Signal Name | Pin Connection | Description |
|---|---|---|---|
| | VDDCORE | 1.65V to 1.95V<br>Decoupling/Filtering capacitors<br>(100 nF and 10µF)(1)(2) | Powers the device.<br><br>Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. |
| | VDDIOM(3) | 3.0V to 3.6V<br>Decoupling/Filtering capacitors<br>(100 nF and 10µF)(1)(2) | Powers External Bus Interface I/O pads.<br><br>Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. |
| | VDDIOP(3) | 3.0V to 3.6V<br>Decoupling/Filtering capacitors<br>(100 nF and 10µF)(1)(2) | Powers Peripheral I/O pads and USB transceivers.<br><br>Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. |
| | VDDOSC | 1.65V to 1.95V<br>Decoupling capacitor (100 nF)(1)(2) | Powers the Main Oscillator. |
| | VDDPLL | 1.65V to 1.95V<br>Decoupling capacitor (100 nF)(1)(2) | Powers the PLL cells. |
| | GND | Ground | GND pins are common to VDDCORE, VDDIOM and VDDIOP pins.<br>GND pins should be connected as shortly as possible to the system ground plane. |
| | GNDPLL | PLL Ground | GNDPLL pin is provided for VDDPLL pin.<br>GNDPLL pin should be connected as shortly as possible to the system ground plane. |
| | GNDOSC | Oscillator Ground | GNDOSC pin is provided for VDDOSC pin.<br>GNDOSC pin should be connected as shortly as possible to the system ground plane. |

| ☑ | Signal Name | Pin Connection | Description |
|---|---|---|---|
| **Clock, Oscillator and PLL** | | | |
| | XIN<br>XOUT<br><br>Main Oscillator<br>in<br>Normal Mode | Crystals between 3 and 20 MHz<br><br>Capacitors on XIN and XOUT<br>(crystal load capacitance dependent)<br><br>1 Kohm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.<br><br>Note: XOUT cannot be used to drive another clock input. | Main Oscillator Internal load capacitance: 20pF<br>Crystal load capacitance to check ($C_{CRYSTAL}$).<br><br>  <br><br>Example: for a 18.432 MHz crystal with a load capacitance $C_{CRYSTAL}$= 25 pF, external capacitors are required: $C_{L1}$= $C_{L2}$ = 2x (25 pF-20 pF - Cboard)<br>If Cboard is about 1.5pF<br>$C_{L1}$= $C_{L2}$= 7pF.<br>Refer to the electrical specifications of the AT91RM9200 datasheet. |
| | XIN<br>XOUT<br><br>Main Oscillator<br>in<br>Bypass Mode | XIN: external clock source<br>XOUT: can be left unconnected | 1.8V square wave signal (VDDOSC)<br>External clock source up to 50 MHz<br>Duty Cycle: 40 to 60%<br>Refer to the electrical specifications of the AT91RM9200 datasheet for $C_{IN}$ and $R_{IN}$ values when using bypass mode. |

| ☑ | Signal Name | Pin Connection | Description |
|---|---|---|---|
| | XIN32<br>XOUT32<br><br>Slow Clock Oscillator | 32.768 kHz Crystal<br><br>External Capacitors:<br>$C_{L1}$ is between XIN32 and Ground<br>$C_{L2}$ is between XOUT32 and Ground<br><br>Note:<br>Wired the 32K crystal as close as possible of the microcontroller. Do not forget to put a guard ring and avoid having any noisy line close to it.<br>XOUT cannot be used to drive another clock input. | Internal parasitic capacitance (including package): 6pF<br>Supported Crystal with a load capacitance ($C_{CRYSTAL}$) from 6pF up to 12.5 pF<br>Maximal External Capacitor:<br>$C_{L1} = C_{L2}$ = 2 x (12.5 - 6 pF - Cboard)= 13 pF- 2xCboard.<br><br>  <br><br>Example: for an 32.768 kHz crystal with a load capacitance of $C_{CRYSTAL}$= 9 pF, Cboard= 1.5 pF, external capacitors are required: $C_{L1} = C_{L2}$ =15pF.<br>Refer to the electrical specifications of the AT91RM9200 datasheet. |

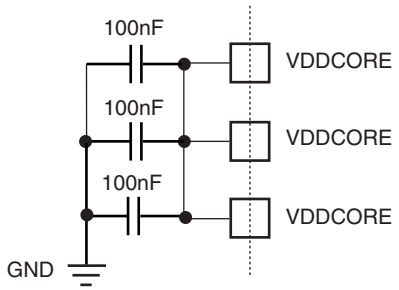
| ☑ | Signal Name | Pin Connection | Description |
|---|---|---|---|
| | PLLRCA<br>PLLRCB | Second-order filter<br><br>Can be left unconnected if PLL not used. | See the Excel spreadsheet:<br>“ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip” (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.<br><br>  <br><br>PLL filter recommendations:<br><br>The Fn parameter represents the cutoff frequency at filter level. The higher the frequency, the better the PLL response time. The user should choose the highest frequency for this parameter, but be aware of the two following constraints:<br>- Increasing Fn decreases the C1 and C2 values at filter level, whereas the resulting C1, C2 values must have values higher than the stray capacitances of the [package + layout].<br>- the Fn frequency must be at least 20 times lower than the input frequency.<br><br>The good damping factor is the one closest to a value of 0.707.<br><br>C1 ~ 10xC2<br><br>R, C1 and C2 must be placed as close as possible to the pins. |

| ☑ | Signal Name | Pin Connection | Description |
|---|---|---|---|
| **ICE and JTAG**[4] | | | |
| | TCK | Connected to ICE/JTAG Interface | This pin is a Schmitt trigger input.<br>Internal pull-up resistor. |
| | TMS | Connected to ICE/JTAG Interface | This pin is a Schmitt trigger input.<br>Internal pull-up resistor. |
| | TDI | Connected to ICE/JTAG Interface | This pin is a Schmitt trigger input.<br>Internal pull-up resistor. |
| | TDO | Connected to ICE/JTAG Interface | Output driven up to $V_{VDDIOP}$ |
| | RTCK | Connected to ICE/JTAG Interface | Output driven up to $V_{VDDIOP}$ |
| | NTRST | To a reset circuitry | NTRST must be driven at power up, even if JTAG port is not used<br>Note: NTRST can be connected to NRST. |
| | JTAGSEL | Must be tied to GND for normal operation and to VDDIOP to use Boundary scan features | This pin is a Schmitt trigger input.<br>Internal pull-up resistor. |
| **Reset/Test** | | | |
| | NRST | Must be connected to reset circuitry. The reset delay must cover the 32Khz start up time (900ms) | This pin is a Schmitt trigger input.<br>Internal pull-up resistor. |
| | TST0, TST1 | These two pins must be connected to ground for normal operation. | |
| | PA31/BMS | Application dependent.<br>Must be tied to VDDIOP to boot from Embedded ROM.<br>Must be tied to GND to boot from external memory.<br>(EBI Chip Select 0). | The BMS signal level during reset time boots from embedded ROM or from a 16-bit parallel Flash.This signal must be stable during reset. |

| ☑ | Signal Name | Pin Connection | Description |
|---|---|---|---|
| **PIO** | | | |
| | PAx<br>PBx<br>PCx | Application dependent. | All PIOs are pulled-up inputs at reset except those which are multiplexed with the Address Bus signals that must be enabled as peripherals:<br>PA30 (A23), PA31 (A24) and PC3 (A25).<br><br>To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled. |
| | PC6/NWAIT | Pull-up (100 KOhm)[(1)] | A pull up is mandatory on NWAIT if this pin in not used.<br>If PC6/NWAIT is driven by an external device, user must ensure that the PC6/NWAIT pin is driven high as soon as the device is powered up. |
| | PDx[(5)] | Application dependent. | ETM features and 2nd USB HOST are available only on PIOD. |
| **Multimedia Card Interface MCI** | | | |
| | PA28/MCCDA | Pull-up to adjust according to MultiMedia Card specification or SD card Part1 physical layer specification | MCIA Command Line |
| | PA8/MCCDB | Pull-up to adjust according to MultiMedia Card specification or SD card Part1 physical layer specification | MCIB Command Line |
| **EBI** | | | |
| | D0-D15<br>(D16-D31) | Application dependent. | Data bus lines D0 to D15 are pulled-up inputs to $V_{VDDIOM}$ at reset.<br><br>Note: Data bus lines D16 to D31 for SDRAM access. D16 to D31 are multiplexed with the PIOC controller.<br>PIO input after reset. |
| | A0-A22<br>(A23-A25) | Application dependent. | Address Bus (A0 to A25)<br>A0 to A22: Address lines are driven to '0' at reset.<br>A23 to A25 Address bus lines are:<br>- multiplexed with the PIOC controller.<br>- PIO input after reset. |
| SMC - SDRAM Controller - CompactFlash® Support | | | |
| See "External Bus Interface (EBI) Hardware Interface" on page 11. | | | |

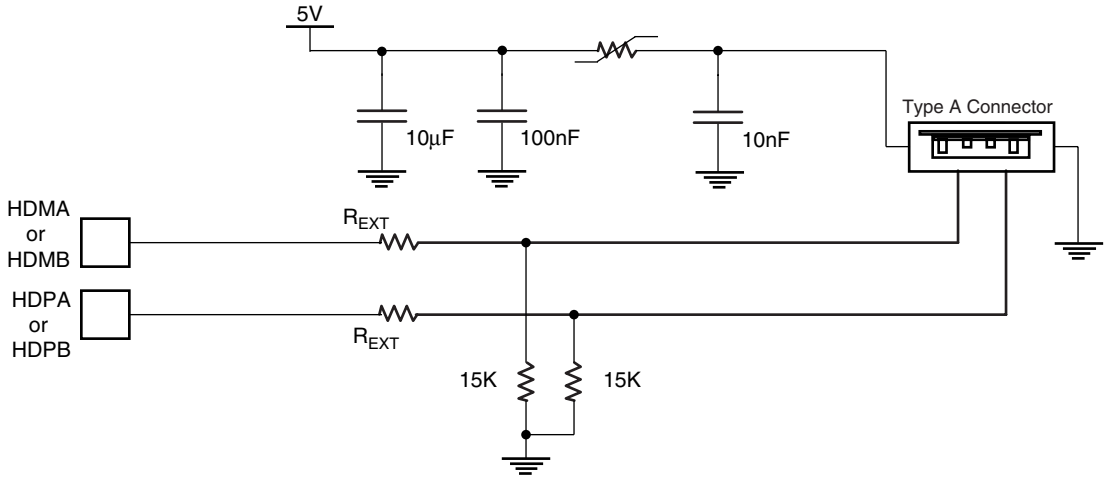
| ☑ | Signal Name | Pin Connection | Description |
|---|---|---|---|
| **USB Host (UHP)** | | | |
| | HDPA<br>HDPB[5] | Application dependent.[6]<br>Typically, 15 kOhm resistor to GND. | No internal pull-down resistors.<br><br>To reduce power consumption, if USB Host is not used, connect HDPA/HDPB to GND. |
| | HDMA<br>HDMB[5] | Application dependent.[6]<br>Typically, 15 kOhm resistor to GND. | No internal pull-down resistors.<br><br>To reduce power consumption, if USB Host is not used, connect HDMA/HDMB to GND. |
| **USB Device (UDP)** | | | |
| | DDP | Application dependent.[7] | No internal pull-down, no internal pull-up resistors.<br><br>To reduce power consumption, if USB Device is not used, connect DDP to VDDIOP. |
| | DDM | Application dependent.[7] | No internal pull-down, pull-up resistors.<br><br>To reduce power consumption, if USB Device is not used, connect DDM to GND. |

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.

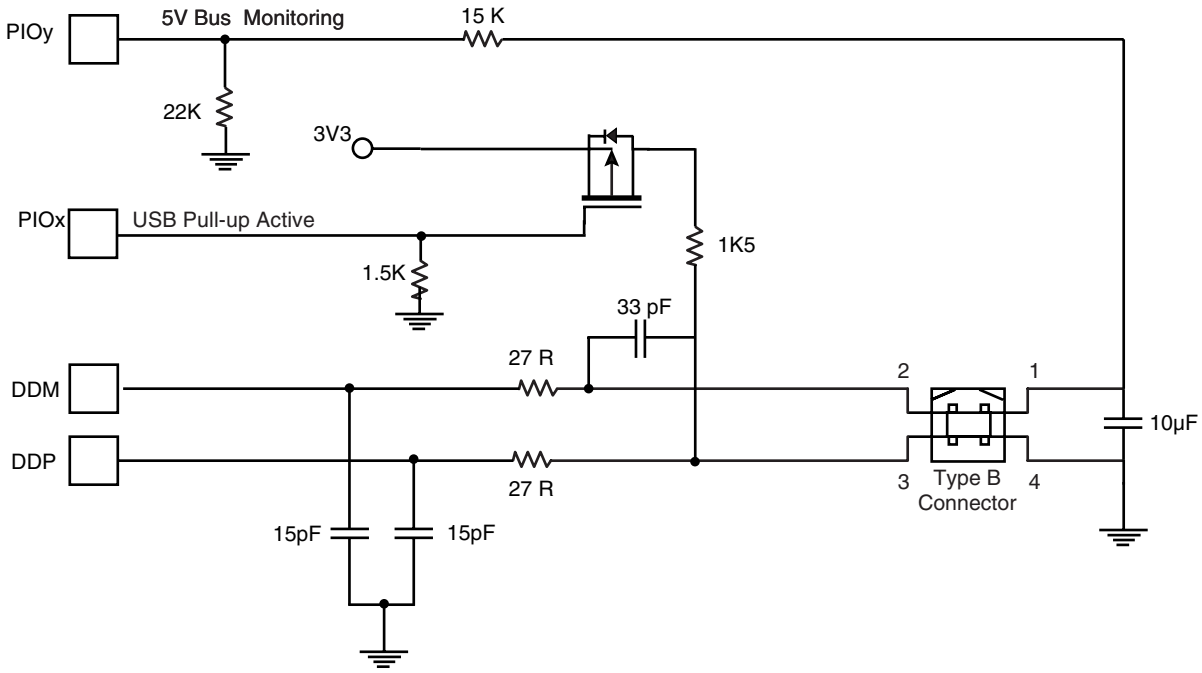



3. The double power supplies VDDIOM and VDDIOP power the device differently when interfacing with memories or with peripherals.
4. It is recommended to establish accessibility to a JTAG connector for debug in any case.
5. Available only in the 256-ball RoHS BGA compliant Package

6. Example of USB Host connection:
A termination serial resistor ($R_{EXT}$) must be connected to HDPA/HDPB and HDMA/HDMB. A recommended resistor value is defined in the electrical specifications of the AT91RM9200 datasheet.




7. Example of USB Device connection:
Pull-up is active by default after reset (required by the boot application). No pull-down: DM is floating when the peripheral is not connected. The application shall monitor VBus and remove the pull-up when the host switch off.



# 4. External Bus Interface (EBI) Hardware Interface

**4.1** Table 4-1 details the connections to be applied between the EBI pins and the external devices for each Memory Controller.

**Table 4-1.** EBI Pins and External Device Connections

| | Pins of the Interfaced Device | | | | | | |
|---|---|---|---|---|---|---|---|
| **Pin** | **8-bit Static Device** | **2 x 8-bit Static Devices** | **16-bit Static Device** | **Burst Flash Device** | **SDRAM** | **CompactFlash** | **NANDFlash/ SmartMedia** |
| **Controller** | **SMC** | | | **BFC** | **SDRAMC** | **SMC** | |
| D0 - D7 | D0 - D7 | D0 - D7 | D0 - D7 | D0 - D7 | D0 - D7 | D0 - D7 | AD0 - AD7 |
| D8 - D15 | – | D8 - D15 | D8 - D15 | D8 - D15 | D8 - D15 | D8 - 15 | – |
| D16 - D31 | – | – | – | – | D16 - D31 | – | – |
| A0/NBS0 | A0 | – | NLB | – | DQM0 | A0 | – |
| A1/NWR2/NBS2 | A1 | A0 | A0 | A0 | DQM2 | A1 | – |
| A2 - A9 | A2 - A9 | A1 - A8 | A1 - A8 | A1 - A8 | A0 - A7 | A2 - A9 | – |
| A10 | A10 | A9 | A9 | A9 | A8 | A10 | – |
| A11 | A11 | A10 | A10 | A10 | A9 | – | – |
| SDA10 | – | – | – | – | A10 | – | – |
| A12 | A12 | A11 | A11 | A11 | – | – | – |
| A13 - A14 | A13 - A14 | A12 - A13 | A12 - A13 | A12 - A13 | A11 - A12 | – | – |
| A15 | A15 | A14 | A14 | A14 | – | – | – |
| A16/BA0 | A16 | A15 | A15 | A15 | BA0 | – | – |
| A17/BA1 | A17 | A16 | A16 | A16 | BA1 | – | – |
| A18 - A20 | A18 - A20 | A17 - A19 | A17 - A19 | A17 - A19 | – | – | – |
| A21 | A21 | A20 | A20 | A20 | – | – | CLE |
| A22 | A22 | A21 | A21 | A21 | – | REG[3] | ALE |
| A23 - A24 | A23 - A24 | A22 - A23 | A22 - A23 | A22 - A23 | – | – | – |
| A25 | A25 | A24 | A24 | A24 | – | CFRNW[1] | – |
| NCS0/BFCS | CS | CS | CS | CS | – | – | – |
| NCS1/SDCS | CS | CS | CS | – | CS | – | – |
| NCS2 | CS | CS | CS | – | – | – | – |
| NCS3/SMCS | CS | CS | C S | – | – | – | – |
| NCS4/CFCS | CS | CS | CS | – | – | CFCS[1] | – |
| NCS5/CFCE1 | CS | CS | CS | – | – | CE1 | – |
| NCS6/CFCE2 | CS | CS | CS | – | – | CE2 | – |
| NRD/NOE/CFOE | OE | OE | OE | – | – | OE | |
| NWR0/NWE/CFWE | WE | WE[4] | WE | – | – | WE | |
| NWR1/NBS1/CFIOR | – | WE[4] | NUB | – | DQM1 | IOR | – |

**Table 4-1.** EBI Pins and External Device Connections (Continued)

| Pin | Pins of the Interfaced Device | | | | | | |
|---|---|---|---|---|---|---|---|
| | 8-bit Static Device | 2 x 8-bit Static Devices | 16-bit Static Device | Burst Flash Device | SDRAM | CompactFlash | NANDFlash/ SmartMedia |
| **Controller** | **SMC** | | | **BFC** | **SDRAMC** | **SMC** | |
| NWR3/NBS3/CFIOW | – | – | – | – | DQM3 | IOW | – |
| BFCK | – | – | – | CK | – | – | – |
| BFAVD | – | – | – | AVD | – | – | – |
| BFBAA/SMWE | – | – | – | BAA | – | – | WE |
| BFOE | – | – | – | OE | – | – | – |
| BFRDY/SMOE | – | – | – | RDY | – | – | OE |
| BFWE | – | – | – | WE | – | – | – |
| SDCK | – | – | – | – | CLK | – | – |
| SDCKE | – | – | – | – | CKE | – | – |
| RAS | – | – | – | – | RAS | – | – |
| CAS | – | – | – | – | CAS | – | – |
| SDWE | – | – | – | – | WE | – | – |
| NWAIT | – | – | – | – | – | WAIT | – |
| Pxx[2] | – | – | – | – | – | CD1 or CD2 | – |
| Pxx[2] | – | – | – | – | – | – | CE |
| Pxx[2] | – | – | – | – | – | – | RDY |

Notes:
1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.
2. Any PIO line.
3. The REG signal of the CompactFlash can be driven by any of the following address bits: A24, A22 to A11.
4. NWR1 enables upper byte writes. NWR0 enables lower byte writes.

# 5. AT91RM9200 Restrictions

## 5.1 Package Restrictions

The AT91RM9200 is available in two packages:

- 208-pin green PQFP, 31.2 x 31.2 mm, 0.5 mm pitch
- 256-ball RoHS compliant BGA, 15 x 15 mm, 0.8 mm ball pitch

The product features of the 256-ball BGA package are extended compared to the 208-lead PQFP package. The features that are available only with the 256-ball BGA package are:

- Parallel I/O Controller D
- ETM™ port with outputs multiplexed only on the PIO Controller D
- a second USB Host transceiver, opening the Hub capabilities of the embedded USB Host.

### 5.2 Multiplexing Restrictions:

The AT91RM9200 features four PIO controllers:

- PIOA and PIOB
  - Multiplexing I/O lines of the peripheral set
- PIOC
  - Multiplexing the data bus bits 16 to 31
  - Several External Bus Interface control signals.
  - Using PIOC pins increases the number of general-purpose I/O lines available but prevents 32-bit SDRAM memory access
- PIOD
  - Available in the 256-ball BGA package option only, multiplexing outputs of the peripheral set and the ETM port

## 6. Internal Boot Program Constraints

- PA31/BMS pin must be set to HIGH level to boot on AT91RM9200 internal boot ROM.
- PLLB must be wired:
  - Associated LFT filter must be optimized for a 96 MHz running frequency with an accuracy of ± 0.25%.

  Use PLL Calculator tools (available on www.atmel.com) to estimate the filter.
- A supported crystal is mandatory between XIN and XOUT (see Table 6-1).
- Supported DataFlash devices (see Table 6-2) connected on NPCS0 or supported EEPROM devices (see Table 6-3).

Note: The main oscillator cannot be bypassed.

See the Boot Program section of the AT91RM9200 datasheet for more details on the boot program.

**Table 6-1.** Supported Crystals (MHz)

| | | | | |
|---|---|---|---|---|
| 3.0 | 3.2768 | 3.6864 | 3.84 | 4.0 |
| 4.433619 | 4.9152 | 5.0 | 5.24288 | 6.0 |
| 6.144 | 6.4 | 6.5536 | 7.159090 | 7.3728 |
| 7.864320 | 8.0 | 9.8304 | 10.0 | 11.05920 |
| 12.0 | 12.288 | 13.56 | 14.31818 | 14.7456 |
| 16.0 | 17.734470 | 18.432 | 20.0 | |

**Table 6-2.** Supported DataFlash Devices

| Device | Density | Page Size (bytes) | Number of Pages |
|---|---|---|---|
| AT45DB011 | 1 Mbit | 264 | 512 |
| AT45DB021 | 2 Mbits | 264 | 1024 |
| AT45DB041 | 4 Mbits | 264 | 2048 |
| AT45DB081 | 8 Mbits | 264 | 4096 |

**Table 6-2.** Supported DataFlash Devices

| Device | Density | Page Size (bytes) | Number of Pages |
|---|---|---|---|
| AT45DB161 | 16 Mbits | 528 | 4096 |
| AT45DB321 | 32 Mbits | 528 | 8192 |
| AT45DB642 | 64 Mbits | 1056 | 8192 |

The DataFlash must be connected to NPCS0 of the SPI.

**Table 6-3.** Supported EEPROM Devices

| Device | Size | Organization |
|---|---|---|
| AT24C16A | 16 Kbits | 16 bytes page write |
| AT24C164 | 16 Kbits | 16 bytes page write |
| AT24C32 | 32 Kbits | 32 bytes page write |
| AT24C64 | 64 Kbits | 32 bytes page write |
| AT24C128 | 128 Kbits | 64 bytes page write |
| AT24C256 | 256 Kbits | 64 bytes page write |
| AT24C512 | 512Kbits | 128 bytes page write |

Generally, serial EEPROMs have no identification code. The bootloader checks for an acknowledgment on the first read. The device address on the two-wire bus must be 0x0. The bootloader supports the devices listed in Table 6-3

## 6.1 Hardware Limitations of the Internal Boot Program

The SPI and TWI drivers use several PIOs in alternate functions to communicate with devices. Care must be taken when these PIOs are used by the application. The devices connected could be unintentionally driven at boot time, and electrical conflicts between SPI or TWI output pins and the connected devices may appear.

Table 6-4 contains a list of pins that are driven during the Boot Program execution. These pins are driven during the boot sequence for a period of about 6 ms if no correct boot program is found. The download through the TWI takes about 5 seconds for 64 Kbytes due to the TWI bit rate (100 Kbits/s).

For the DataFlash driven by the SPCK signal at 12 MHz, the time required to download 64 Kbytes is reduced to 66 ms.

**Table 6-4.** Pins Driven during Internal Boot Program Execution

| Peripheral | Pin | PIO Line |
|---|---|---|
| SPI | MOSI | PA1 |
| SPI | SPCK | PA0 |
| SPI | NPCS0 | PA3 |
| TWI | TWD | PA25 |

**Table 6-4.** Pins Driven during Internal Boot Program Execution

| | | |
|---|---|---|
| TWI | TWCK | PA26 |
| DBGU | DRXD | PA9 |
| DBGU | DTXD | PA10 |

The AT91RM9200 Boot program supports serial communication via the DBGU or DFU protocol via the USB Device Port. The USB pull-up must be active by default after reset.

## 7. External Boot Constraints

PA31/BMS pin must be set to LOW level.

Boot from an external 16-bit parallel Flash connected on NCS0.

All initialization (PLL,SDRAM, SMC, etc.) is user dependent.

# 8. Revision History

**Table 8-1.** Revision History

| Doc. Rev | Comments | Change Request Ref. |
|---|---|---|
| 6323A | First issue | |

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